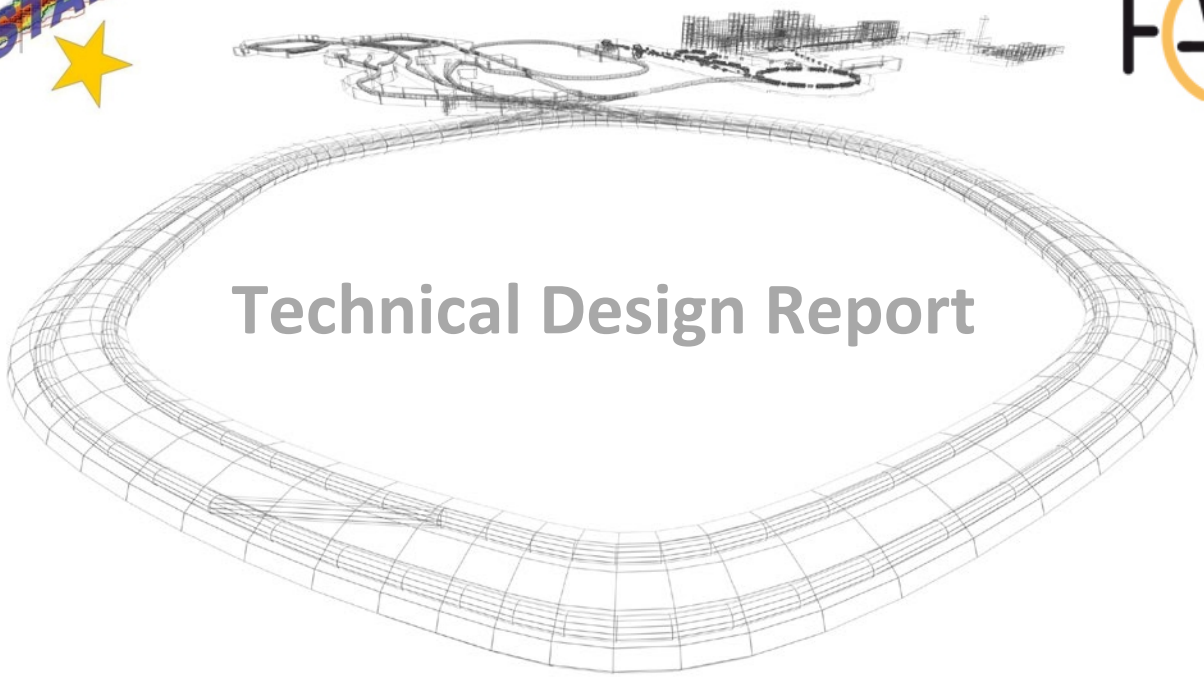
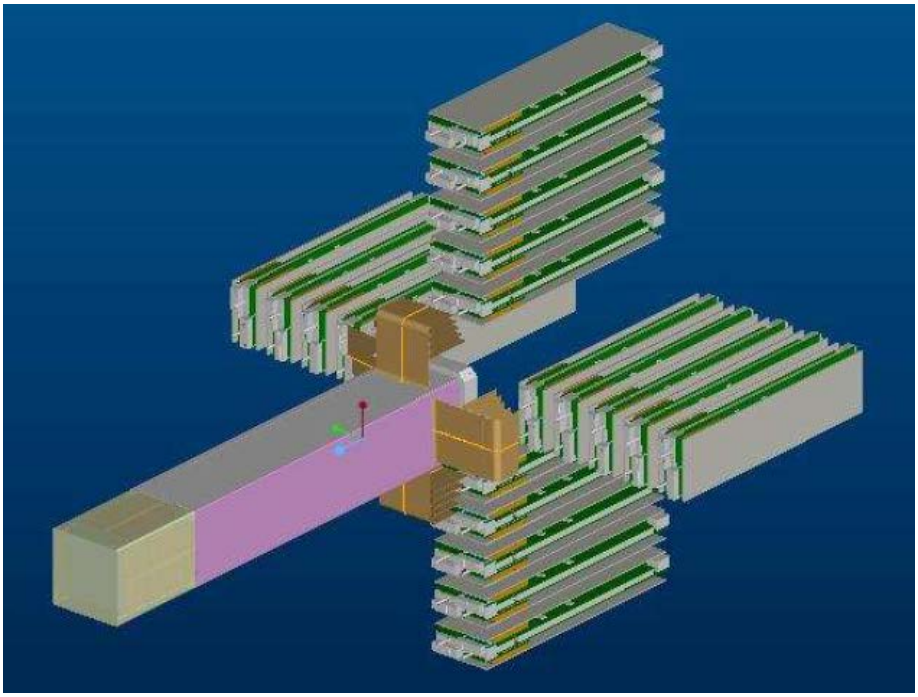


Technical Design Report

Technical Report
for the Design, Construction and Commissioning of the Advanced Implantation Detector Array (AIDA)



Technical Report For the Design, Construction and Commissioning of the Advanced Implantation Detector Array (AIDA)

November 2008

Abstract

The Advanced Implantation Detector Array project is a silicon detector array designed for implantation-decay correlation measurements for exotic nuclei produced by the SuperFRS. The project has been fully funded by the UK. Specification has been completed and detailed design is underway. Prototype hardware will be available for test in 2009.

1 AIDA Collaboration

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2 Introduction and overview

The objective of the Advanced Implantation Detector Array (AIDA) project is to develop, commission and exploit a state of the art silicon detector array for decay spectroscopy experiments using the SuperFRS fragment separator at FAIR. It is anticipated that AIDA will be operated standalone and in conjunction with other DESPEC collaboration detection systems, such as gamma-ray and neutron detector arrays, which requires that AIDA should be very compact and use minimum material while still accepting all ions from the fragment separator.

To achieve these objectives AIDA will use large area double-sided silicon strip detector (DSSSD) and application specific integrated circuit (ASIC) technologies. AIDA will be used for implantation-decay experiments and perform spectroscopy quality measurements of charged particle decays with energies from tens of keV to MeV. The challenge is to achieve this within microseconds of multi-GeV exotic ion implants and with an instrumentation density to match the very high degree of detector segmentation required for the observation and characterisation of long-lived decays.

This project is fully funded by the UK Science & Technology Facilities Council (STFC) by grants to each of the AIDA collaborators. The project commenced August 2006 and prototype detectors and instrumentation will be available for in-beam tests in 2009, to be followed by production detectors and instrumentation in 2010.

3 Physics requirements for subsystem

3.1 Implantation-Decay Correlation

Very high energy ($\sim 100-200$MeV/u, $A \leq 240$ ions), very exotic heavy-ions are implanted into a stack of double-sided silicon strip detectors (DSSSDs). These nuclei subsequently undergo radioactive decay emitting low energy β-particles, protons, α-particles, neutrons and γ rays. The charged particles are detected by the DSSSDs. The detector systems are schematically illustrated in figure 1

The DSSSD strips identify where (x, y) and when (t_0) the nuclei were implanted. Subsequent radioactive decay(s) at the *same* position (x, y) at times $t_1(, t_2 \ldots)$ can be correlated with the implant. Observation of a number of such correlations enables the determination of the energy distribution of the radioactive decay and its half-life.

If the implantation events are distributed across a highly segmented DSSSD the average time between implants at each position (x, y) is greater than the average decay time and random correlations are minimised. For a given decay time, higher segmentation means a higher total implantation rate.

3.2 Practicalities

The energy deposited by the implant in the DSSSD is $\sim$GeV, and higher. The energy of the subsequent decay events is $\sim$MeV. Average time between implantation and decay is

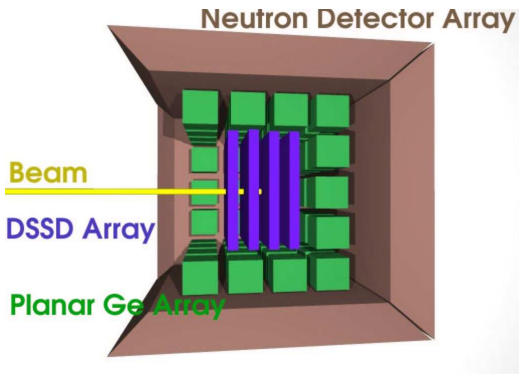

Figure 1: Conceptual illustration of the DEcay SPECtroscopy (DESPEC) detector systems.

$\sim \mu$s$-$s.

We cannot assume that it will be possible to preempt the arrival of high energy implants by, for example, using external signals to switch the preamplifiers to reset. The instrumentation must detect, respond and recover autonomously.

DSSSD array area is $\sim$24cm$\times$8cm. Each layer of DSSSD stack consists of multiple, 1mm thick, DSSSD wafers with a junction and ohmic strip pitch of $\sim$ 600μm. Strips on one side of the DSSSD wafer are series connected. The stack may consist of 1 to many DSSSD layers. It is anticipated that this detector will be used in 'cocktail' mode, i.e. many different species of ion will be implanted across the detector in conjunction with a gamma-ray and ToF neutron detector arrays.

A second configuration will have an array area of $\sim$8cm$\times$8cm (common DSSSD wafer design and therefore common segmentation). It is anticipated that a single species will be implanted across the detector in conjunction with the 4π neutron detector or the Total Absorption Spectrometer (TAS).

The heavy-ion implants will induce significant and relatively rapid performance degradation due to radiation damage, i.e. the detectors will require periodic replacement. The instrumentation will therefore be separated from the detector and effectively shielded by its enclosure and cooling system, and by the material of the other detector systems.

3.3 Required Capabilities

- Selectable Gain
  high ∼20MeV Full Scale Range (FSR) **OR** intermediate ∼1GeV FSR

  AND

  low ∼20GeV FSR (via separate overload recovery signal processing)
  energy measurement of implantation and decay events

- Selectable threshold $< 0.25 - 10\%$ FSR Minimum threshold <50keV @ high gain
  $\Rightarrow$ rms noise <5keV assuming threshold = 5σ
  observe and measure low energy betas, beta detection efficiency

- Integral $< 0.1\%$ and differential non-linearity $< 2\%$ for $> 95\%$ FSR
  spectrum analysis, calibration, threshold determination

- Autonomous overload detection and recovery $\sim \mu$s
  observe and measure fast implantation-decay correlations

- Nominal signal processing time $< 10\mu$s
  observe and measure fast decay-decay correlations

- Receive(transmit) time-stamp data
  correlate events with data from the DAQs of other detector sub-systems (gamma and neutron detector arrays, upstream tracking detectors)

- Timing trigger for coincidences with other detector systems
  time resolution < BUTIS clock period (5ns)
  minimise random correlations, DAQ rate management, neutron ToF

4 Technical specification and design details

4.1 Double Sided Silicon Strip Detector (DSSSD)

4.1.1 DSSSD Wafer

- DC design
- Common biasing to p^+n junction and n^+n ohmic strips via integrated polysilicon resistors (15 ± 5)MΩ
- Detector thickness 1000μm
- 8cm × 4cm ($4''$ wafer technology)
- 128×64 strips (8cm × 4cm)

- Strip pitch $\sim 600\mu$m
- Inter-strip distance 50μm (consistent with obtaining $> 10^7$MΩ resistance between n^+n ohmic strips)
  $\Rightarrow\sim 85\%$ of detector area is active
- Multiple guard rings for both p^+n junction and n^+n ohmic sides of the wafer
- Dead space (passivation, guard rings, common bias line and polysilicon bias resistors) surrounding active area ≤ 1.5mm
- Operating bias ≤ 200V
- Typical wafer leakage current $1-5$nA/cm$^2/100\mu$m (20°C) at operating bias $\Rightarrow 0.64-3.2\mu$A for 8cm $\times$ 8cm area and 1000μm thickness
- Maximum (8cm $\times$ 8cm) wafer leakage current $< 5\mu$A (20°C) at operating bias
- Maximum strip leakage current $<$ 100nA (20°C) at operating bias
- 100% of strips functional to above specification

Operating bias is defined as the voltage required to obtain maximum charge collection and equivalent resolution for p^+n junction *and* n^+n ohmic strips for α-particles, whether incident on the junction or ohmic strips.

4.1.2 DSSSD Package

- Two package types: (i) 24cm $\times$ 8cm using (6 off 4cm $\times$ 8cm wafers) with series bonded n^+n strips, (ii) 8cm $\times$ 8cm using (2 off 4cm $\times$ 8cm wafers) with series bonded n^+n strips
- FR4 transmission PCB mounting
- Flexible Kapton PCB cabling directly bonded to PCB
- Tri-plate (ground/signal/ground planes) flexible Kapton PCB
- Flexible Kapton PCB length $\sim$60cm
- PCB design to permit (i) use at any position in DSSSD stack, (ii) use at 0° or 180° with respect to an axis normal to the surface of the detector and other DSSSD planes in the stack
- PCB design to include thermocouple connection point
- PCB dimensions $\sim$ 26cm $\times$ 10cm $\times$3mm, $\sim$ 10cm $\times$ 10cm $\times$3mm,

4.1.3 Planned DSSSD Procurement

- 1 off prototype 24cm × 8cm detector
- 1 off prototype 8cm × 8cm detector
- 9 off production 24cm × 8cm detectors
- 9 off production 8cm × 8cm detectors

4.2 Intrinsic Resolution Limits of Silicon Detectors

The term intrinsic detector resolution refers to the response of a detector to a mono-energetic source of radiation and assumes that we can neglect the effects of dead layer, recombination, trapping and incomplete charge collection.

For β-particles we assume that the energy resolution will be equivalent to the electronic noise of the instrumentation. For protons and α-particles we assume that the energy resolution will be the quadratic sum of the statistics of the ionisation process, the effects of nuclear collisions at the end of the particle track and the electronic noise. Statistics: for 1MeV protons and 5MeV α-particles the contributions are 1.5keV FWHM and 3.4keV FWHM respectively. Collisions: for protons and α-particles the contributions are 0.7keV FWHM and 6.3keV FWHM respectively. For 1MeV protons and 5MeV α-particles the quadratic sums of the statistical and collisional contributions are 2.3keV FWHM and 7.2keV FWHM respectively. Unless the electronic noise is significantly lower than 12keV FWHM (1400e^- rms), the intrinsic detector resolution will be dominated by the electronic noise. If we assume (i) a resolution of 12keV FWHM, (ii) that data from discrete (Gaussian) peaks should be spread over 4 channels FWHM (for accurate centroid determination) and (iii) that the high gain range corresponds to 20MeV FSR then this implies 13-bit ADCs.

For heavy-ions ($A \geq 12$) the intrinsic energy resolution will be completely dominated by the effects of nuclear collisions at the end of the particle track and charge collection effects arising from the high density charge deposition. Lindhard and Neilson (Phys. Lett. 2 (1962) 209) estimate the contribution from nuclear collisions as

$$\Delta E_{\text{coll}}(\text{keV FWHM}) = 0.7 Z^{\frac{1}{2}} A^{\frac{4}{3}} \tag{1}$$

which ranges in value from ∼0.8MeV (^{58}Ni) to ∼10MeV (^{238}U).

4.3 Implantation Event Characteristics

The maximum energy loss of heavy-ions in 1mm of silicon (normal incidence):

Ion	$\Delta E_{\max}$ (GeV)
^{58}Ni	3
^{120}Sn	7
^{238}U	17

The maximum energy that can be deposited in 1mm of silicon at, or near, normal incidence is therefore $\leq$20GeV which establishes the FSR requirement for the high-energy signal processing instrumentation.

Range of heavy-ions in silicon as a function of incident energy (normal incidence):

	Range (mm)			
Ion	50MeV/u	100MeV/u	200MeV/u	300MeV/u
^{58}Ni	1.0	3.3	11.8	20.9
^{120}Sn	0.8	2.3	7.1	13.7
^{238}U	0.6	1.7	4.7	8.9

Calculations performed using SRIM-2003 (http://srim.org). To implant ions at a distance of $3-5$mm into the DSSSD stack requires energies of $\sim 100-200$MeV/u.

Multi-GeV implants are expected to result in data from a cluster of strips for each DSSSD plane traversed by the ion. It is expected that $\sim$5 adjacent p^+n junction and $\sim$5 adjacent n^+n ohmic strips per DSSSD plane will produce data per event with the majority of the energy to be found at the cluster centre.

The energy and spatial distribution for the incoming implantation ions will be determined by the properties of the SuperFRS, low-energy branch (LEB) and any degraders, tracking detectors, AIDA entrance window etc. We assume that ions of a given A/q will be implanted across the DSSSD planes with a Gaussian transverse profile ($\sigma_x = \sigma_y \sim 1$cm) and a depth distribution ($\sigma_z \sim 1-2$mm). We assume implantation rates across the 24cm $\times$ 8cm DSSSD plane of $\sim$ 10kHz, with peak rates for ions with a given $A/q \sim$ 1kHz. If we wish to observe lifetimes $\sim$s then this implies a segmentation of $\sim$ 0.5mm $\times$ 0.5mm.

The observables of interest are:

- position/track of implant
  p^+n and n^+n strip numbers
- absolute energy of implant
  to $\sim 0.1\%$ precision

- implant time
  for time correlation with respect to (i) subsequent charged-particle decay events and (ii) isomeric decays detected by other detector arrays, precision (per event) 5ns

- time of implant
  by prompt trigger, precision < 5ns

4.4 Decay Event Characteristics

Typical decay event for protons (energy $0.5 - 2$MeV, range $7 - 50\mu$m) and α-particles (energy $3 - 12$MeV, range $15 - 100\mu$m) will consist of one p^+n junction strip and one n^+n ohmic strip from one DSSSD plane. A fraction of events (inter-strip area:total area) will occur between strips and these events will typically be 1 or 2 adjacent p^+n junction strip(s) and 1 or 2 adjacent n^+n ohmic strip(s). In addition, for those decays due to implants close ($< 100\mu$m) to the surfaces of the DSSSDs it is possible for the decay to have sufficient energy to escape one DSSSD plane and be stopped in another. These events would therefore consist of data from two DSSSD planes with the event structure for each DSSSD plane as described above.

β-particles of interest will have energies in the range from $\sim$tens of keV to > 10MeV (range >25mm) - a large fraction of the β-particles of interest will not be stopped in one DSSSD plane. In addition, there is a significant probability that the β-particles will be scattered by the silicon. Events can therefore consist of data from multiple adjacent strips and DSSSD planes. There will be inter-strip events as described above.

The observables of interest are:

- position of decay
  p^+n and n^+n strip numbers

- absolute energy of charged-particle decay
  centroid of energy distribution of multiple decays to $\ll 1$LSB

- absolute energy of threshold
  β detection efficiency, to 1LSB

- decay time
  for time correlation with respect to previous implantation events or charged-particle decays, precision (per event) 5ns

- time of decay
  by prompt trigger for time of flight (ToF) measurements, precision < 5ns

4.5 Radiation Damage

The MSL type BB/5 DSSSD (area 32mm $\times$ 32mm, thickness $\sim 70\mu$m) is used for implantation decay experiments using the Fragment Mass Analyser (FMA) at the Argonne

National Laboratory. These detectors continue to provide useful data with leakage currents $\leq 5\mu$A at ~ -10°C. Scaling by area and thickness to the AIDA DSSSD we could expect a leakage current of $\sim 450\mu$A per 8cm $\times$ 8cm wafer or $\sim 3\mu$A per strip at ~ 0°C. This per strip leakage current would correspond to $\sim$50keV FWHM of noise for a shaping time $\tau = 1\mu$s: the noise would vary as $\sqrt{\tau}$ (see Appendix A). This might be sufficient for some measurements of α and proton decays but it would compromise low threshold detection of β-particles as the threshold would need to be increased to $\sim$110keV (5σ).

The above considerations indicate that it would be advantageous to cool the DSSSDs to a temperature significantly below 0°C. Because the silicon wafers are attached to the detector PCB using an electrically conductive epoxy the lower temperature limit is ~ -20°C. The DSSSDs and their mounting will need to be designed to ensure good thermal contact to achieve and maintain the temperatures required. Thermocouples to measure the temperature of the mounting and DSSSD PCB temperature will also be required.

Caveats The MSL type BB/5 is used with $40 - 80$MeV $A = 100 - 200$ ions which have a range significantly less than the thickness of the silicon wafer - damage is localised in depth (whereas for AIDA DSSSDs it will be more uniformly distributed through the wafer thickness) and therefore the scaling probably underestimates the leakage current of the AIDA detector. The MSL type BB/5 detector bias is usually set at $\times 3 - 5$ the depletion voltage - this is significantly higher than we will be able to achieve with the AIDA DSSSD, therefore the scaling probably overestimates the leakage current of the AIDA detector. This might also indicate that we will not be able to achieve equivalent charge collection and therefore resolution with the lower electric field of the 1000μm AIDA DSSSDs and therefore not be able to operate at equivalent levels of radiation damage.

4.5.1 Mitigation strategies

- Rotate detector layers - distribute radiation dose
- Detector cooling - leakage current reduction, improved charge collection
- Increased detector bias - improved charge collection
- Instrumentation physically separated from DSSSDs

4.6 Application Specific Integrated Circuit (ASIC)

A schematic diagram of ASIC functionality is shown in figure 2.

4.6.1 Low-energy channel ($0 - 20$MeV)

Preamplifier

- Differential input, with adjustable operating point, for optimum performance for both polarities of charge

- Feedback capacitor $\sim$ 1pF, with feedback stabilisation circuit (equivalent to a high-value resistor)
- Input referred noise 1400e$^-$ rms = 12keV FWHM (Si), preferably lower
- Adjustable operating point, for optimum performance with both positive and negative charge
- Integral non-linearity $< 0.1\%$.

Shaper

- Variable shaping time ($\sim 0.5 - 5\mu$s), to minimise ballistic deficit
  Risetime variations $< 0.05\tau$ to maintain ballistic deficit effects $< 0.1\%$ assuming $CR - RC$ shaping (K.Hatch, IEEE Trans. Nucl. Sci. NS15 (1968) 303).
- $\sim$ 1V range of output voltage
- Integral non-linearity $< 0.1\%$

Slow amplifier/comparator

- Bandwidths matched to shaper (to avoid adding noise)
- Amplifier with $\times$10 gain before comparator, to minimise effect of offset variations
- Usable threshold range 50keV$-$2MeV ($0.25 - 10\%$ full-scale)
- Low end of threshold determined by offsets and noise - desirable to achieve 25keV

Fast comparator

- Signal taken straight from pre-amp output, without band-limiting
- Timing resolution <5ns, but with high noise (unsuitable for operation with low thresholds)
- Direct connection to control logic, to provide high-speed digital timing pulse should be OR'd with slow comparator output

Peak-hold

- Rectifying current mirror architecture (to maintain output linearity)
- Low-leakage design, for good stability
  Assume 1V FSR, 14-bit ADC $\Rightarrow$ 1LSB = 61μV
  Droop $\ll$1LSB, 0.1LSB say $\Rightarrow$ droop $< 6\mu$V per readout cycle ($< 10\mu$s)

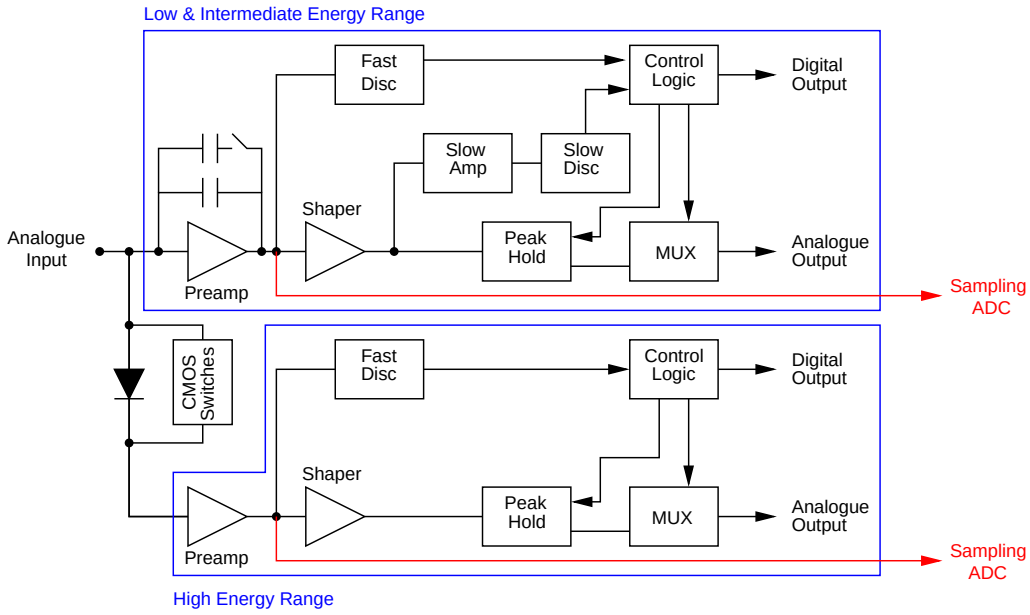

Figure 2: Schematic diagram of the functionality of one ASIC channel

4.6.2 Intermediate energy channel $(0 - 1\mathbf{GeV})$

Preamplifier feedback $\sim$ 50pF. Scale noise, minimum threshold etc. from low energy $(0 - 20\text{MeV})$ specification.

4.6.3 High-energy channel $(0 - 20\mathbf{GeV})$

Pre-amp

- Similar to low-energy design, but optimised for $\sim$ 1nF feedback capacitor
- Large current flow in amplifier output transistors (needs to exceed the peak current from the detector)
- Input referred noise $\sim 5 \times 10^6 \text{e}^-\text{rms}$, $\sim$50MeV FWHM (Si).

Diode and CMOS switches

- Diode to connect high-energy amplifier to detector when low-energy channel saturates
- CMOS switches connected in parallel with diode, after saturation has been detected
- Switches to be reset, after the charge has been integrated by the high-energy amplifier

Fast shaper, Peak-hold, Fast comparator: As before. Minimum threshold $< 2\%$ FSR. Fast shaper noise not constrained by shaping time. Slow amplifier/comparator: Omitted (noise performance is not so critical for the higher energies)

4.6.4 Control Logic

This block manages the link between the peak-hold circuits and the multiplexers. The stored voltages from the peak-holds are accessed in sequence, whenever over-threshold conditions are detected. The logic will also handle the reset of analogue circuitry, including the CMOS switches. The intention is to minimise the recovery time from high-energy pulses - the target is a few microseconds.

The multiplexers will provide analogue voltages over a 1V range for the external ADC. It will be possible to provide a reference voltage, so the ADC can operate in fully differential mode. The reference voltage will match any drift of the active multiplexer outputs, for example variations with temperature or power supply.

4.6.5 Overload Recovery

The effect of the 20GeV implant in the detector is to cause a rapid change of voltage on the amplifier inputs for the channel. The low-energy amplifier goes into saturation, and the signal charge is immediately coupled to the high-energy amplifier. The coupling is initially via a forward-biased diode, but the connection is maintained by CMOS switches until the high-energy amplifier has completed the integration of the charge.

The next step is to disconnect the high-energy amplifier and to reset the low-energy amplifier. This will speed up the recovery from the implant event, giving sensitivity to decay products within a few microseconds. The reset could be implemented by switched feedback components in the amplifier, and probably in the low-energy shaper as well. It will not be necessary to wait many shaper time-constants before the signal baseline is recovered.

It is important for the reset process to be clean - it must not create spurious charge injection which might trigger the low-energy comparators. This could be achieved by a time-sequence of reset pulses which allows the amplifier and shaper to recover fully before the comparator becomes active.

4.6.6 Package

ASIC channel pitch to be compatible with strip pitch of DSSSD ($\sim 600\mu$m). 16 (c. 10mm $\times$ 6mm) channels per ASIC.

4.6.7 ASIC Production Requirements

Each 24cm$\times$8cm DSSSD requires 512 channels of instrumentation (384 p^+n strips, 128 n^+n strips). Each 8cm$\times$8cm DSSSD requires 256 channels of instrumentation (128 p^+n strips, 128 n^+n strips).

To evaluate the prototype ASIC with a fully instrumented 8cm$\times$8cm DSSSD would require a minimum of 16 (size c. 10mm $\times$ 6mm) operational dies. To evaluate the prototype ASIC with a fully instrumented 24cm$\times$8cm DSSSD would require a minimum of 32 (size c. 10mm $\times$ 6mm) operational dies.

For the production ASIC, ten DSSSDs will require 5120 channels of instrumentation which implies a minimum of 320 (size c. 10mm $\times$ 6mm) operational dies.

4.7 Front End Electronics (FEE)

The FEE will provides an integrated instrumentation and data acquisition system. The ASICs will be wire bonded to a mezzanine PCB which will be attached to the front end of the FEE. The ASIC signals will be buffered and digitised by ADCs and the digital data will be processed by an Field Programmable Gate Array (FPGA). Data will be transmitted from the FEE by a Gbit ethernet interface.

A diagram illustrating the FEE card concept and functionality is shown in figures 3 and 4. Each FEE card will support 64 channels of instrumentation.

Preamplifier differential inputs - p^+n/n^+n and reference voltage (reference voltage varied depending what type of strip is connected to other pin) means that FEE cards can be used for either p^+n junction or n^+n ohmic strips.

4.7.1 ADC

The ADC will be the Analog Devices AD976A 200kSPS, 16-bit ADC. Power dissipation $<$ 100mW.

For the prototype ASIC design, it will be possible to connect a sampling ADC directly to the output of the charge sensitive preamplifier to evaluate the use of digital signal processing instead of the more conventional shaper, peak detect & hold and ADC configuration. Potential advantages include the ability to measure decay-decay correlations to $\sim$100ns, pulse shape analysis, ballistic deficit corrections etc. The ADC will be the Analog Devices AD9252-50 Octal, 50MSPS, 14-bit ADC. Power dissipation 93.5mW per channel. SOIC package 64-pin LFCSP_VQ size $\sim$9mm $\times$ 8.9mm.

4.7.2 FPGA

Xilinx Virtex 5 (with PowerPC core running Linux) for control, data processing, event building. Integrated Gbit ethernet port.

4.7.3 Other

- Power supply regulators and filtering.
- ROM for FPGA configuration data.
- Gbit ethernet driver.
- Estimated FEE PCB size 80mm $\times$ 300mm.
- Power dissipation 25W per FEE PCB.

- Each FEE PCB to have a unique, electronically readable, identification number. This will enable (i) the use of *ab initio* calibrations/parameters/corrections determined during laboratory bench acceptance tests, (ii) the monitoring of operational parameters for effects such as radiation damage.

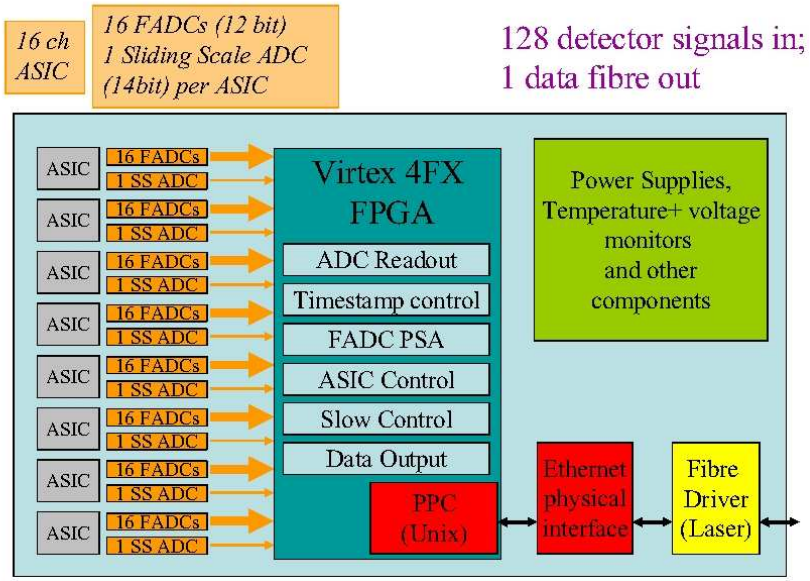

Figure 3: Front End Electronics (FEE) concept

4.7.4 FEE Production Requirements

Each 24cm×8cm DSSSD requires 512 channels of instrumentation (384 p^+n strips, 128 n^+n strips). Each 8cm×8cm DSSSD requires 256 channels of instrumentation (128 p^+n strips, 128 n^+n strips). Each FEE card provides 64 channels of instrumentation.

To evaluate the prototype ASIC with a fully instrumented 8cm×8cm DSSSD would require a minimum of 4 FEE cards. To evaluate the prototype ASIC with a fully instrumented 24cm×8cm DSSSD would require a minimum of 8 FEE cards.

For production, ten 24cm×8cm DSSSDs will require a minimum of 80 FEE cards.

4.7.5 Data Acquisition (DAQ)

A diagram illustrating the DAQ concept and functionality is shown in figure 5

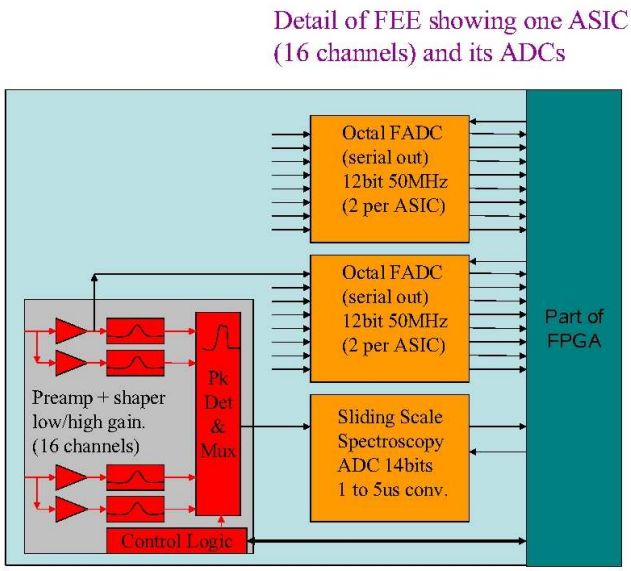

Figure 4: Front End Electronics (FEE) concept showing detail for one ASIC

- Data acqusition architecture compatible with NUSTAR DAQ standard.
- BUTIS link to AIDA via local interface.

4.7.6 Slow Control Interface

- Web-based interface (SOAP)
- Control and parameter history to be available as strip chart (cf. EPICS at TRIUMF).

4.7.7 ASIC Control

The controls required include ASIC gain, shaping time, threshold controls per channel, power supplies. Parameters to be included in data stream with a timestamp on a periodic basis

4.7.8 Subsystems Control

Controls required include:

- AIDA DSSSD bias, voltage/current trip, voltage set point, ramp rate
- Coolant recirculator (on/off/set point)
- Vacuum pump (on/off)

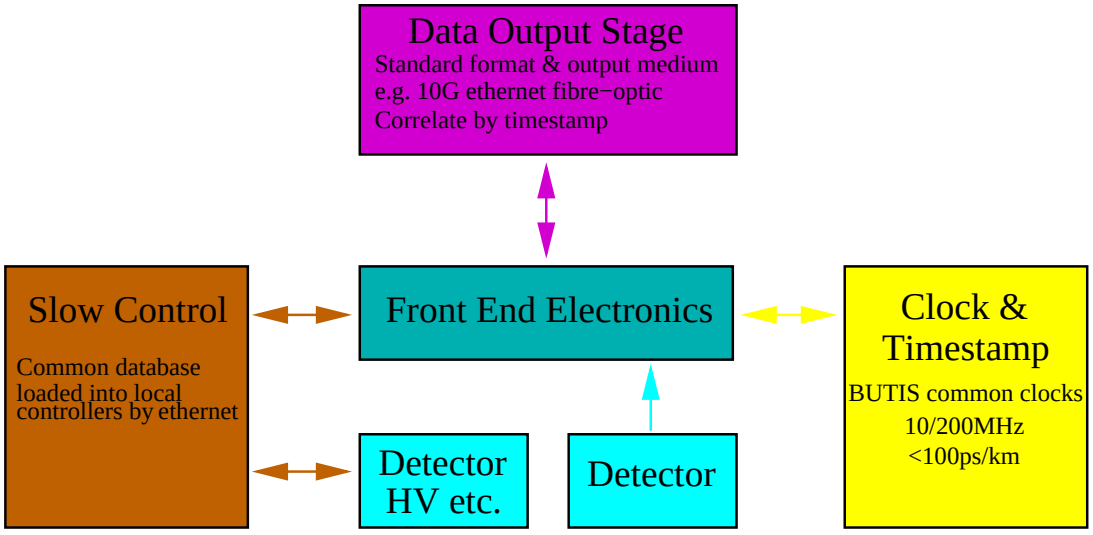

Figure 5: NUSTAR Data Acquisition (DAQ) concept

Parameters to be included in data stream with a timestamp on a periodic basis

- Accelerator parameters of interest
- SuperFRS parameters of interest
- AIDA DSSSD bias, leakage current, status (on/off/over-voltage/over-current/fail/trip)
- Coolant recirculator status, operating temperature
- AIDA DSSSD mounting block, DSSSD PCB temperatures
- AIDA DSSSD enclosure pressure
- FEE PCB ID numbers

4.7.9 Systems Integration

AC Coupling

- For full-scale response (20MeV=1V FSR) in one high gain channel, we require $<$ 0.25% FSR ($<$ 2.2fC) response in adjacent channels. Coupling capacitance between adjacent channels is (see appendix)

$$24\text{cm} \times 1.6\text{pF/cm} + 20\text{pF} = 58\text{pF} \tag{2}$$

So strip voltage fluctuation is given by

$$\delta V \leq \frac{Q}{C} \leq \frac{2.2\text{fC}}{58\text{pF}} \leq 38\mu\text{V} \tag{3}$$

To achieve this voltage fluctuation the coupling capacitance required is

$$C_c \geq \frac{\text{FSR}}{\delta V} C_f \geq \frac{1\text{V}}{38\mu\text{V}} 1\text{pF} \geq 26\text{nF} \tag{4}$$

The nearest decade value is 22nF.

- Assuming a 22nF coupling capacitor, a full-scale response for an intermediate gain channel (1GeV = 1V FSR, $C_f = 50$pF) will be accompanied by a voltage fluctuation of

$$\delta V = \frac{1\text{V}}{440} = 2.3\text{mV} \tag{5}$$

on the detector strip. This will inject charge

$$\delta Q = \delta V \times 58\text{pF} = 0.13\text{pC} \tag{6}$$

which corresponds to 0.3% crosstalk.

- Assuming a 22nF coupling capacitor, a full-scale response for a low gain channel (20GeV = 1V FSR, $C_f = 1$nF) will be accompanied by a voltage fluctuation of

$$\delta V = \frac{1\text{V}}{22} = 45\text{mV} \tag{7}$$

on the detector strip. This will inject charge

$$\delta Q = \delta V \times 58\text{pF} = 2.6\text{pC} \tag{8}$$

which corresponds to 3% crosstalk.

- Require 22nF/200V+ coupling capacitor per channel
  Required rating exceeds nominal rating of capacitors arrays (typically 100V) but laboratory tests of production samples indicate that these devices can be operated at the biases required.
- Ceramic, low $1/f$ noise
- Locate on kapton cabling connector PCB.

Detector Bias

- Voltage $\leq$ 500V, current $\leq$ 3mA per DSSSD plane
- Polarity positive and negative
- Bias configuration (see figure 6)
- Noise $\leq 1.2\mu$V rms (bandwidth defined by instrumentation)
  Should be negligible contributor to total noise. Assume total noise of 12keV FWHM $\Rightarrow$ noise contribution $\leq$ 3keV FWHM, $\leq 350e^-$ rms

$$\delta V \leq \frac{Q}{C_D} \leq \frac{350 \times 1.6021 \times 10^{-19}}{46 \times 10^{-12}} \leq 1.2\mu\text{V rms} \tag{9}$$

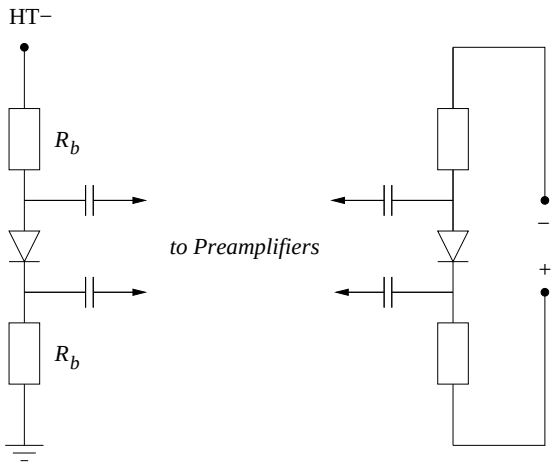

Figure 6: Detector bias options

4.7.10 Detector Enclosure and Cooling

Cooled, dry, inert gas will be recirculated inside the detector enclosure at a pressure of ∼1.1 bar.

4.7.11 Instrumentation Cooling

The power density of the FEE card mandates the use of water cooling (see Mechanical design subsection).

4.7.12 Current Status and Outstanding Issues

The DSSSD is currently in the tendering process with prototypes required for mid-2009.

The ASIC design has reached an advanced stage and the prototype submission to AMS is imminent. Design simulations indicate that in most respects the prototype ASIC will meet, or exceed, design specifications. Two areas of concern are the minimum threshold and timing performance.

Detailed design simulations have shown that variances in component values will result in offsets to the comparators comparable to the minimum threshold required ($<$ 50keV at high gain). To workaround this issue the ASIC design includes progammable comparator input offsets. Further optimisation of the design of the production ASIC will incorporate the experience and results obtained from the prototype ASICs.

The timing performance required of AIDA by the ToF array is 400ps rms at minimum threshold - a very challenging specification. Detailed transient analysis indicates that for a 50keV threshold at high gain the time resolution will be 2.7ns rms (200keV) and 0.13ns rms (20MeV). Note these figures will degrade with radiation damage due to increased shot noise. It should also be noted that they do not include detector effects. Again we are at the limit of what simulations can usefully tell us and we have elected to proceed with the

current design. We intend to further optimise the design using the experience and results obtained from the prototype ASICs and DSSSD.

The design concept and overall layout of the FEE card is now established and detailed design and layout is underway.

4.7.13 Further Information

Further detailed information on the technical specifications can be found at:
`http://www.ph.ed.ac.uk/ td/AIDA/Design/design.html`

4.8 Mechanical

4.8.1 Design Control

The mechanical design of AIDA will be a controlled document held by CCLRC Daresbury Laboratory. This document will define the position of, and space required by, AIDA. It will therefore define the space *not available* to other DESPEC and SuperFRS systems. The mechanical design document will be made available to the DESPEC collaboration via the web (URL to be provided).

4.8.2 Installation

The AIDA system will be installed on rails to permit routine transfer to/from the in-beam position.

4.8.3 Materials

Detector enclosure material types and thicknesses selected to minimise γ ray attenuation and neutron absorption. The current options are an aluminium alloy or aluminized carbon-fibre. Detailed design work is underway to determine the thickness and structure required for each material for evaluation by other DESPEC groups which will be impacted by the material budget.

4.8.4 Design

Figures 8 and 9 illustrate the current design concept. This design concept is also compatible with current plans for the 4π neutron detector and TAS.

5 Radiation environment, safety issue

Detector test and energy calibration will require the use of calibration sources (10kBq).

The cooling of the detectors by recirculating gas will require a small (we require a volume of 10 litres at near atmospheric pressure) gas bottle of dry, inert gas (e.g. Argon).

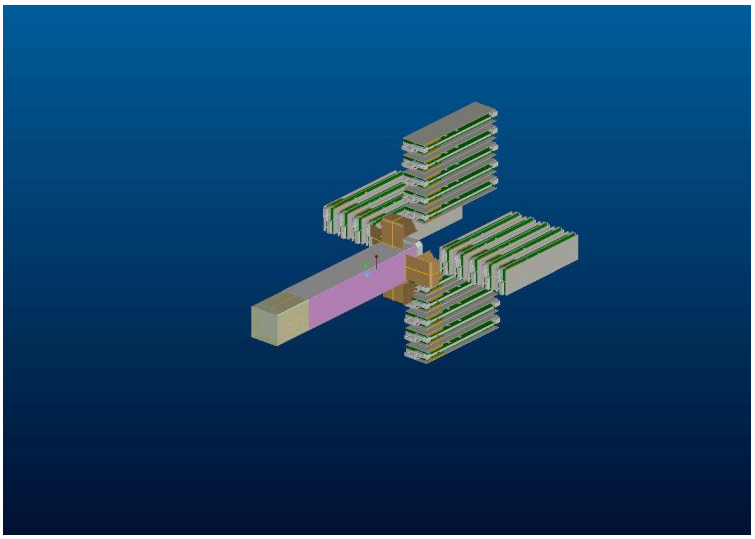

Figure 7: AIDA detector enclosure for 8cm×8cm DSSSDs with FEE cards

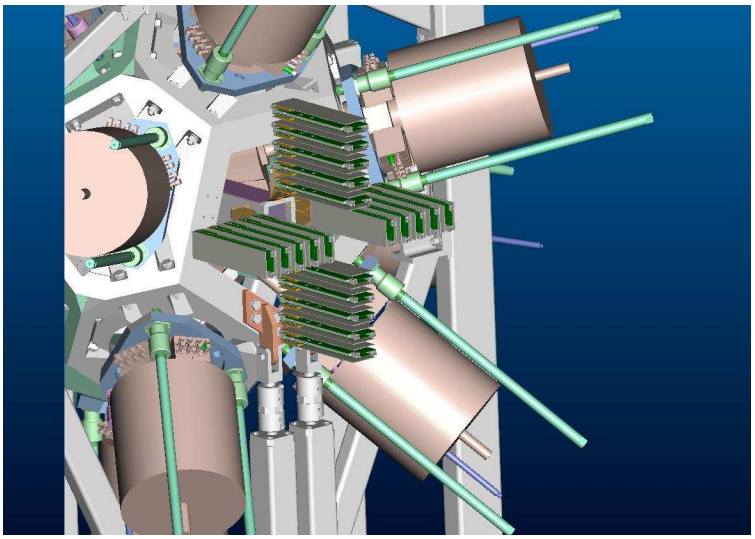

Figure 8: AIDA detector enclosure for 8cm×8cm DSSSDs with FEE cards shown in relation to RISING.

6 Production, Quality Assurance and Acceptance Tests

All production AIDA system components will be tested with respect to their specification in the UK by the AIDA collaboration prior to delivery to FAIR. Upon delivery, further tests will be conducted by the AIDA collaboration to verify safe delivery and compatibility with other DESPEC detector systems and FAIR infrastructure.

7 Civil engineering, cave, cooling, cranes etc.

The principal requirements for the infrastructure of the experimental area are:

- Electrical power for experimental equipment only with high quality ground reference (single point grounding)
- Water as coolant for FEE
- Dedicated Gbit network infrastructure for experimental data transfer and experiment control

8 Installation procedure, its time sequence, necessary logistics from A to Z including transportation

To be defined.

9 Cost and funding

The AIDA project is fully funded by the UK STFC. In terms of deliverables to FAIR (including detectors, instrumentation, power supplies, mechanical support structure, computer and network hardware etc.) the total value is estimated to be 975kEuro.

10 Time schedule table and Milestones

- EPSRC grant submission: January 2006
- EPSRC physics prioritisation panel: April 2006
- Project commencement: August 2006
- ASIC prototype design submission: January 2009
- Prototype DSSSD, ASIC & FEE available: July 2009
- Production DSSSD, ASIC & FEE: July 2010
- Experimental programme commencement: 2010/11

11 Organization and distribution of responsibilities

Responsibility for major sub-tasks are distributed amongst AIDA collaborators as follows:

- DSSSD University of Edinburgh
- ASIC STFC Rutherford-Appleton Laboratory
- FEE STFC Daresbury Laboratory
- Software STFC Daresbury Laboratory
- Mechanical Design STFC Daresbury Laboratory and University of Liverpool
- Mechanical Construction University of Liverpool
- Support Infrastructure University of Liverpool
- Systems Integration STFC Rutherford-Appleton Laboratory, STFC Daresbury Laboratory and University of Liverpool
- Test & Commissioning University of Edinburgh and University of Liverpool

Thsi distribution reflects the particular expertise and capabilities of each of the AIDA collaborators.

AIDA collaboration meetings are held monthly at the STFC Rutherford-Appleton Laboratory and STFC Daresbury Laboratory to review and discuss progress. Progress reports and outstanding issues are discussed with the wider DESPEC collaboration during bi-annual collaboration meetings. All AIDA collaboration materials can be found at the AIDA collaboration website:

`http://www.ph.ed.ac.uk/ td/AIDA`